MS-I

FACILITY FORM 602

N66-13525	
(ACCESSION NUMBER)	(THRU)
17	1
(PAGES)	(CODE)
CR 68712	08
(NASA CR OR TMX OR AD NUMBER)	(CATEGORY)

SEL

systems engineering laboratories, incorporated

FINAL REPORT

NAVIGATION SYSTEM TEST STATION

Prepared for

NATIONAL AERONAUTICS
AND
SPACE ADMINISTRATION

GEORGE C. MARSHALL
SPACE FLIGHT CENTER

Huntsville, Alabama

Under Contract
Number NAS 8-11584

SEL SYSTEMS ENGINEERING LABORATORIES, INCORPORATED
P. O. BOX 9148 • FORT LAUDERDALE, FLA. 33310 • AREA CODE 305 587-2900

CONTENTS

ILLUSTRATIONS

FINAL REPORT

1. GENERAL

This documentation contains a final report on two Navigation System Test Stations designed and manufactured by Systems Engineering Laboratories, Incorporated, Fort Lauderdale, Florida. The test stations were designed to meet the specific requirements of the National Aeronautics and Space Administration at the George C. Marshall Space Flight Center in Huntsville, Alabama under contract NAS 8-11584.

1.1 Purpose of Equipment

The test stations are controlled by a RCA110A computer and perform test and measurement functions on several configurations of navigation systems within the Saturn Program.

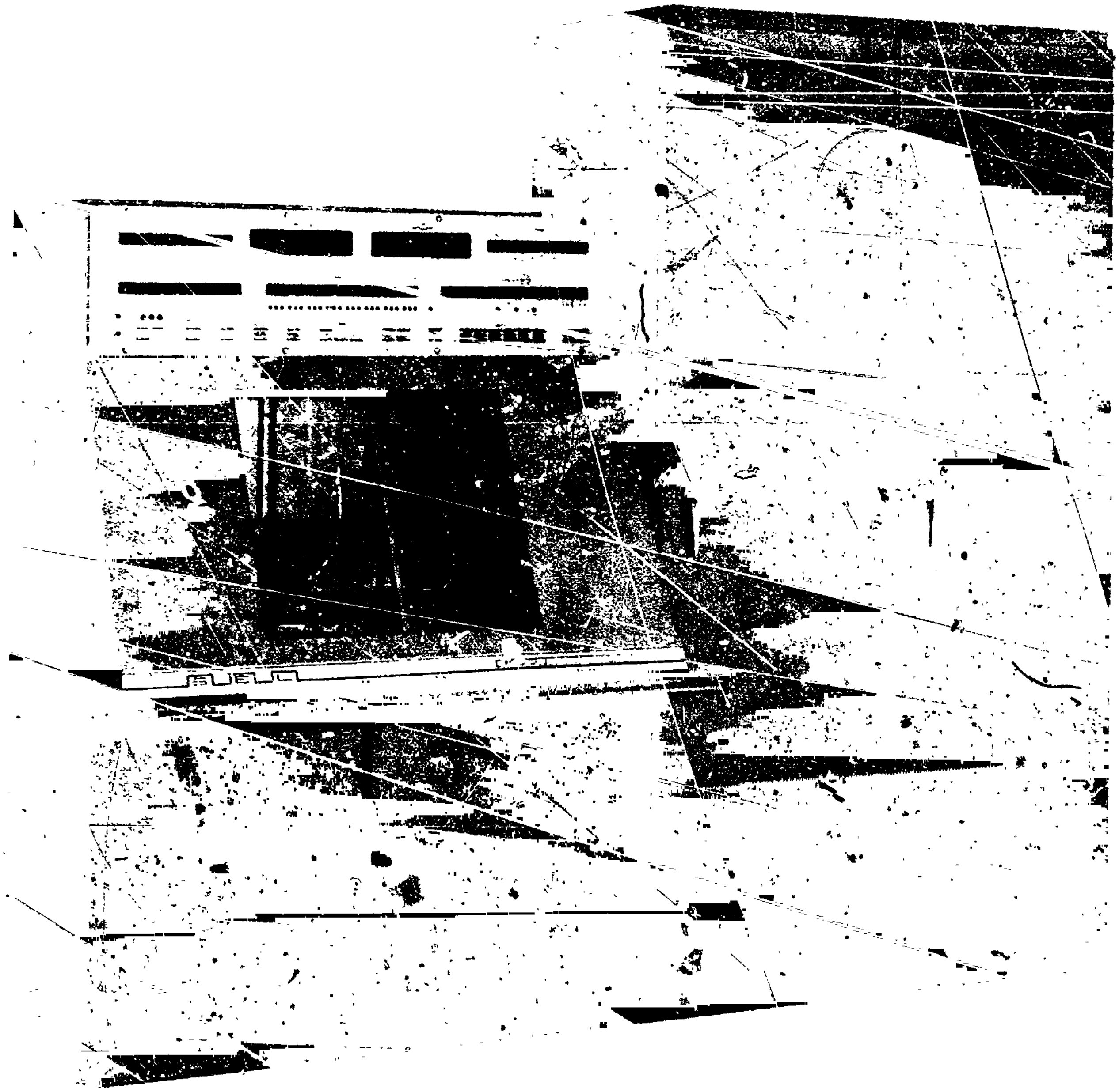
1.2 Description and Characteristics

a. General

Each test station consists of a buffer and control section and a measurement section. A photograph of one of the test stations is shown in Figure 1-1. The buffer and control section consists of an input register with a parity checker, an output register with a parity generator, an electric typewriter with control logic, station operating controls and displays and system timing and control logic. The measurement section consists of a 64-channel DC solid state multiplexer, a 120-channel DC relay multiplexer, a 60-channel AC relay multiplexer with an AC to DC converter, an analog-to-digital converter, 22 DC level detectors, 12 DC voltage level alarms, 10 AC voltage level alarms, 32 signal output relays with a select register and matrix, and 64 recorder relays with a select register and matrix. A block diagram which illustrates the logical arrangement of the units is shown in Figure 1-2.

Transformer isolated cable drivers drive the wire transmission link between the computer and test station. One set of drivers, located in the buffer and control console, drive the signals from the test station to the computer. A second set, located approximately 30 feet from the computer, drive the command signals from the computer to the test station. The drivers are capable of driving signals through lines up to 1000 feet in length. All lines between the test station and computer are DC isolated.

Flip-flops are used in all buffer registers and counters. Standard NOR logic is used for all decoding, parity generating and checking, and all control logic functions. Logic levels are 0 (ZERO) and -6 (ONE) volts.



N2010

Figure 1-1 Navigation System Test Station

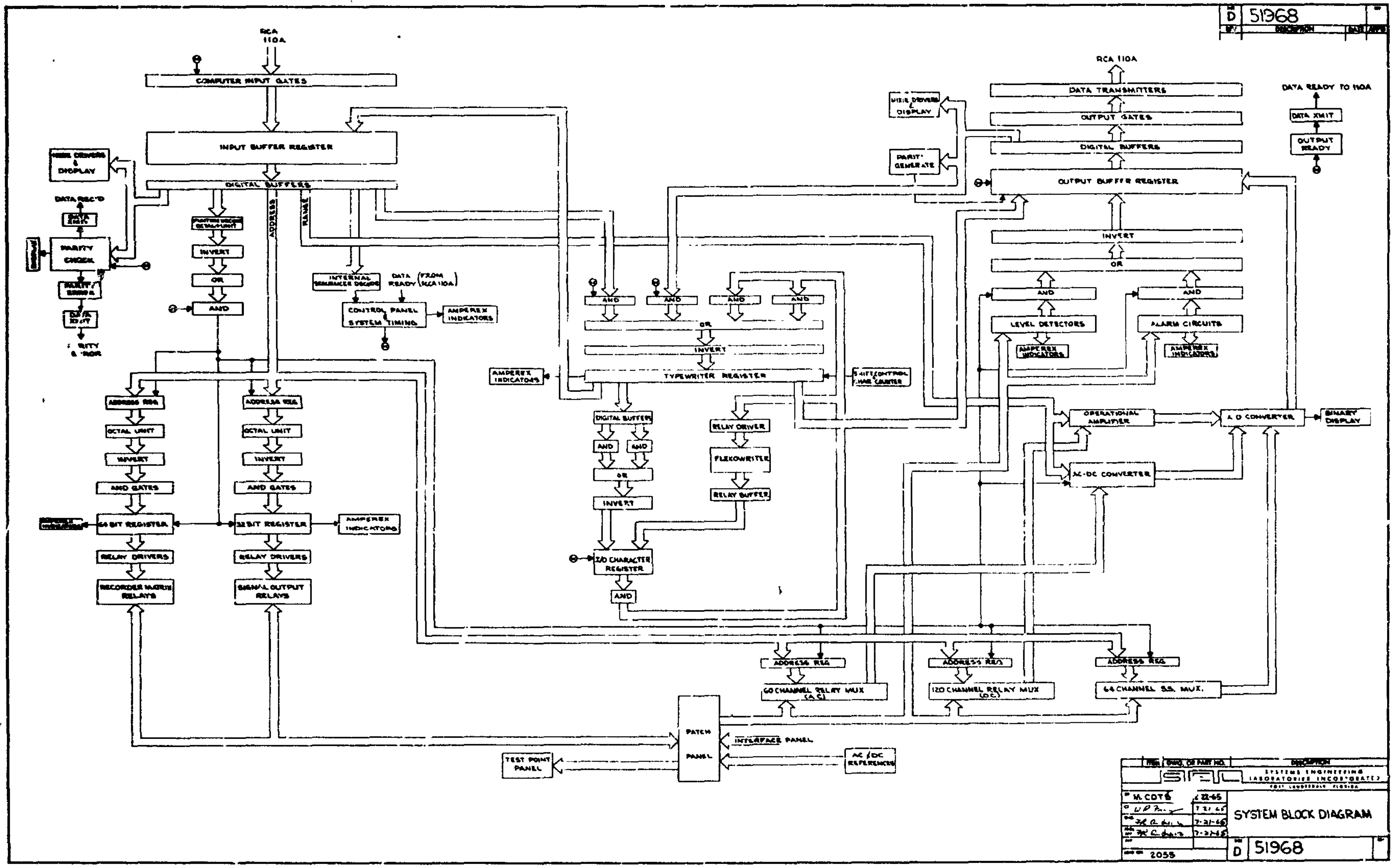


Figure 1-2 Block Diagram-Navigation System Test Station

All back lighted switches consist of Master Specialities actuators and display units with Micro-switch switch units. Amperex 6977 Triode Indicators are used for binary displays and Nixie tubes are used for octal displays. All primary operating controls and indicators are located on a sloping panel across the top of the console.

All analog and digital circuits are designed by Systems Engineering Laboratories (SEL) and are packaged on epoxy/glass printed circuit cards measuring 3.25 by 5 inches. The circuit cards are mounted in slide-out card trays using Elco plug-in connectors. All wiring connections to the connectors are accomplished using the "wire-wrap" technique. All wiring connections between the trays, with the exception of the multiplexers and A/D converters, are accomplished with multi-pin Amp Series M connectors. The wire-wrap connections, plug-in circuit cards and multi-pin connectors eliminate most soldering operations during modification, maintenance or repair.

The pull-out card trays are mounted in the cabinets on ball-bearing slides. A wire bundle at the rear of each tray is encased in a protective metal sleeve. The card trays can be extended when power is applied, and when they are extended, all circuit test points and adjustments are readily available. Additional information on the card trays and circuit cards can be found in Section II (Component Designations and Circuit Card Descriptions). All cabinets are equipped with RFI shielding.

Access doors on the front and rear of each cabinet and the pull-out logic trays allow easy access to the equipment. All wiring between the major assemblies is routed in plastic channels with protective covers. Electrical outlets are provided on the AC power distribution panels as power sources for test equipment.

b. Functional Description

(1) Word Format

The operating sequence of the test station is determined from a 24-bit input control word. The word format is shown in Figure 1-3. The 24 bits are designated 0 through 23 and each group of three bits are combined to form one octal character. The eight octal characters are designated 1 through 8.

The test station function is determined by the bits in octal characters 6 and 7. A function decode unit detects which bits are present to generate the appropriate command signal. Logic is provided to detect a total of 23 different command signals (octal codes 01 through 07, 10 through 17 and 20 through 27). The individual commands are listed in tabular form in Figure 1-3.

Octal characters 3, 4 and 5 contain address information which selects an individual signal output or recorder matrix relay or an individual

24-BIT INPUT WORD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8 OCTAL DIGITS	8			7			6			5			4			3			2			1		
	P	SPARES		TEST STATION FUNCTION						ADDRESS SELECT									RANGE			INTERNAL SEQUENCER INSTR.		

5 4 3	2 1 0	
0 0 1	0 1 0	END OF MESSAGE

2	1	0		
0	0	0	0	No instruction.
0	0	1	1	Print message from computer
0	1	0	2	Print word from output
0	1	1	3	Spare
1	0	0	4	Light execute switch
1	0	1	5	Reset buffer.
1	1	0	6	Reset station
1	1	1	7	Enter message for computer

5	4	3		DC MEASUREMENT
0	0	0	0	Spare
0	0	1	1	±0.512V = Full Scale
0	1	0	2	±1.024V = Full Scale
0	1	1	3	±10.24V = Full Scale
1	0	0	4	±20.48V = Full Scale
1	0	1	5	±61.44V = Full Scale
1	1	0	6	Spare
1	1	1	7	Spare

5	4	3		AC MEASUREMENT
0	0	0	0	Spare
0	0	1	1	1.024V = Full Scale
0	1	0	2	10.24V = Full Scale
0	1	1	3	51.20V = Full Scale
1	0	0	4	153.60V = Full Scale
1	0	1	5	Spare
1	1	0	6	Spare
1	1	1	7	Spare

14	13	12	11	10	9	8	7	6		
0	0	0	0	0	0	0	0	0	000	SIGNAL SELECT (RELAYS 1-32)
			THROUGH							
0	0	0	0	1	1	1	1	1	037	
0	0	0	1	0	0	0	0	0	040	AC RELAY MULTIPLEXER (CHANNELS 1-60)
			THROUGH							
0	0	0	1	1	1	0	1	1	073	
0	0	0	1	1	1	1	0	0	074	SOLID STATE MULTIPLEXER (CHANNELS 1-64) OR RECORDER SELECT (RELAYS 1-64)
0	0	0	1	1	1	1	0	1	075	
0	0	0	1	1	1	1	1	0	076	
0	0	0	1	1	1	1	1	1	077	
0	0	1	0	0	0	0	0	0	100	DC RELAY MULTIPLEXER (CHANNELS 1-120)
			THROUGH							
0	0	1	1	1	0	1	1	1	167	
0	0	1	1	1	1	0	0	0	170	392 SPARE ADDRESS SELECT CODES
			THROUGH							
1	1	1	1	1	1	1	1	1	777	

20	19	18	17	16	15		
0	0	0	0	0	0	00	Spare
0	0	0	0	0	1	01	Solid state multiplexer.
0	0	0	0	1	0	02	DC relay multiplexer.
0	0	0	0	1	1	03	Level inputs
0	0	0	1	0	0	04	Alarms.
0	0	0	1	0	1	05	Set signal output relay.
0	0	0	1	1	0	06	Reset signal output relay.
0	0	0	1	1	1	07	Reset all signal output relays.
0	0	1	0	0	0	10	AC relay multiplexer - Direct TVM
0	0	1	0	0	1	11	AC relay multiplexer - Direct FVM.
0	0	1	0	1	0	12	AC relay multiplexer - Direct IPVM.
0	0	1	0	1	1	13	AC relay multiplexer - Direct QVM.
0	0	1	1	0	0	14	AC relay multiplexer - Floating TVM.
0	0	1	1	0	1	15	AC relay multiplexer - Floating FVM
0	0	1	1	1	0	16	AC relay multiplexer - Floating IPVM.
0	0	1	1	1	1	17	AC relay multiplexer - Floating QVM.
0	1	0	0	0	0	20	Interrogate break point switches.
0	1	0	0	0	1	21	Set recorder relay.
0	1	0	0	1	0	22	Reset recorder relay.
0	1	0	0	1	1	23	Internal sequencer instruction.
0	1	0	1	0	0	24	Reset all recorder relays.
0	1	0	1	0	1	25	Select phase A reference.
0	1	0	1	1	0	26	Select phase B reference.
0	1	0	1	1	1	27	Select phase C reference.
0	1	1	0	0	0	30	40 SPARE FUNCTION CODES
	THROUGH						
1	1	1	1	1	1	77	

23	22	21		
0	-	-	0	NO PARITY BIT
0	-	-	1	
0	-	-	2	
0	-	-	3	- = SPARE BIT
1	-	-	4	PARITY BIT
1	-	-	5	
1	-	-	6	
1	-	-	7	

Figure 1-3. Input Control Word Format (Octal Mode)

A1223

multiplexer channel. The address select information is gated to one of several address registers depending upon the test station function. For example: if the test station function is 02, the address select information is gated into the address register for the 120-channel DC relay multiplexer. The individual recorder matrix relay, signal output relay, AC relay multiplexer channel or solid state multiplexer channel is selected in the same manner.

Octal character 2 contains range information for the AC to DC converter or operational amplifier. A decode unit determines which bits are present in the character and provides a signal which determines the full scale output of the converter or amplifier. If the test station function is code 02 (DC relay multiplexer), the range information is applied to the operational amplifier. If the test station function code is any one of codes 10 through 17 (AC relay multiplexer), the range information is applied to the AC to DC converter. The full scale inputs of the amplifier and converter are listed in Figure 1-3. Full scale output is ±10.24 volts.

Octal character 1 contains internal sequence instruction information which also controls the operation of the test station. The individual instructions are listed in Figure 1-3. Internal sequencer instructions 1 and 7 can be performed only if the test station function code is 23.

Octal character 8 contains parity information for the 24-bit word. The two least significant bits (21 and 22) of the character are spares. The most significant bit contains a parity bit when the total number of ONES in the remaining 23-bits (0 through 22) is an even number

(2) Input Data Display

Input display logic encodes each 24-bit word into eight octal characters which are displayed by Nixie indicators on the control panel. The Nixies are designated ISI, RANGE, CHANNEL ADDRESS (3), FUNCTION (2) and PARITY. The PARITY Nixie displays a number of 4 if the parity bit (23) contains a ONE.

(3) Input Parity Check

Input parity check logic monitors each input word to determine if the word contains an even or odd number of ONES. When the parity is correct (ODD) during the automatic or single step modes, a data received signal is gated to the computer. If the parity is incorrect, the data received signal and a parity error signal are gated to the computer. The parity error signal also lights a PARITY lamp on the control panel, and inhibits any output from the test station function decode logic. The system remains locked up until another data ready signal is received from the computer.

When an internal sequencer instruction command 1 (print word from computer) is received, a data received signal is automatically transmitted to the computer regardless of the parity. If the parity is in error, the parity error lamp does not light. All outputs from the parity check logic are inhibited during the manual mode of operation.

(4) Operating Modes

The test station can be operated in the automatic, single step or manual mode. During the automatic or single step mode, 24-bit control words from the computer are loaded into the input buffer register upon receipt of a data ready signal. During the manual mode, the control words are generated by selecting the desired eight octal characters on the typewriter and providing an input command. As each character is selected, it is coded into a 3-bit octal code which is shifted into the typewriter input/output register. When the input command is provided, the 24-bit word is gated into the input register. The input command is generated by selecting the "i" key on the typewriter. During the automatic or manual mode, the desired function is performed automatically after the word is entered into the input register. During the single step mode, the function is not performed until the operator provides an "EXECUTE" command.

Simultaneous with the parity check, octal characters 6 and 7 are decoded to generate the function command. The function command gates, when applicable, the address, range and sequencer instruction information to the appropriate portions of the logic and starts the main system timing. The main system timing logic is not started if a parity error is detected. After distribution, the timing logic generates the necessary internal commands to perform the function and, if applicable, to load the generated or obtained data into the output register. If a word is loaded into the output register, parity information for that word is generated and a data ready signal is transmitted to the computer. The system then remains in a quiescent state until a data received signal is received from the computer. The data received signal clears the data from the output lines.

(5) Recorder Relays

A total of 64 three-pole relays are provided. Three-wire signal lines (signal, ground and shield) from the patch panel are connected to the normally open contacts of each relay (192 wires). When the relay is energized, the input signal is applied through the poles of the relay. The poles of each group of eight relays are bussed together, therefore only eight sets of lines (24 wires) exist between the poles of the relays and 4F8 - P21.

When a "set recorder relay" function command (21) is loaded into the input register, the function decode logic provides a signal to gate the address select information into the address register. The outputs of the address register are applied to decode logic which provides simultaneous octal units and tens output signals. These output signals set one of 64 flip-flops (one per relay). One output of the flip-flop energizes the associated relay and provides an inhibit signal which prevents setting any of the other seven flip-flops which control those seven relays which are common to the selected relay. A second output of the flip-flop lights an Amperex indicator. The relay is de-energized and the Amperex indicator is turned off by resetting the flip-flop. The flip-flop is reset by re-applying the same address information but changing the function command to "reset recorder relay" (22). All previously energized relays can be de-energized by applying a function command of "reset all recorder relays" (24) which resets all previously set flip-flops. Separate indicators are provided for each relay. A test switch is provided to simultaneously test all indicators. The indicators and test switch are located on the maintenance panel, 3F7.

(6) Signal Output Relays

A total of 32 three-pole relays are provided. Three-wire signal lines (signal, ground and shield) from the patch panel are connected to the poles of each relay (96 wires). Two sets of three-wire signal lines, one from the normally closed contacts and one from the normally open contacts, exist between the contacts of the relays and the patch panel. When one of the relays is energized, the input signal to the poles of the relays is switched from one set of outputs to a second set of outputs.

When a "set signal output relay" function command (05) is loaded into the input register, the function decode logic provides a signal to gate the address select information into the address register. The outputs of the address register are applied to decode logic which provides simultaneous octal units and tens output signals. These output signals set one of 32 flip-flops (one per relay). One output of the flip-flop energizes the associated relay. A second output of the flip-flop lights an Amperex indicator. The relay is de-energized and the Amperex indicator is turned off by resetting the flip-flop. The flip-flop is reset by re-applying the same address information but changing the function command to "reset signal output relay" (06). All previously energized relays can be de-energized by applying a function command of "reset all signal output relays" (07) which resets all previously set flip-flops. A separate indicator is provided on the control panel for each relay. A TEST switch momentarily lights all indicators. A SET switch sets all control flip-flops to energize all relays. A CLEAR switch resets all flip-flops to de-energize all relays.

(7) Solid State Multiplexer

The solid state multiplexer is commanded each time a test station function code of 01 is received. The multiplexer samples the channel indicated by the information in the address select bits of the input word. The multiplexer can be commanded at a maximum rate of 10,000 commands per second and the individual channels can be selected at random. Following receipt of the command, the address bits are gated into the address register to select the input channel. The selected channel is sampled by activating an electronic switch (Bright) and the sample is presented to the analog-to-digital converter. A total of 64 input channels are provided and input signals may range from -10.24 to +10.24 volts DC.

(8) Relay Multiplexers

The DC relay multiplexer gates any one of 120 DC voltage signals from the patch panel to the analog-to-digital converter. When a "DC relay multiplexer" function command (02) is received, the function decode logic provides a signal to gate the address and range information into the appropriate registers and to start the main system timing. The outputs of the address register are decoded to energize one of 120 relays which causes the input signal to be applied to an operational amplifier. Range decode logic provides an output signal which controls the gain of the operational amplifier. The output of the amplifier is applied to the analog-to-digital converter. The data inputs to the multiplexer may range from 0 to ±61.44 volts. The individual channels may be sampled at random at any rate up to 400 samples per second.

The AC relay multiplexer gates any one of 60 AC voltage signals from the patch panel to the analog-to-digital converter. The AC relay multiplexer is commanded in much the same manner as the DC relay multiplexer, however, the individual samples are applied to an AC to DC converter. The range information controls the full scale output of the AC to DC converter which is applied to the analog-to-digital converter. The inputs may range from 0 to 153.6 volts rms and the individual channels may be sampled at any rate up to 5.0 samples per second.

The AC relay multiplexer is commanded by any one of function codes 10 through 17 (octal). Function codes 10 through 13 cause direct voltage inputs to be sampled. Function codes 14 through 17 cause floating voltage inputs to be sampled. A function code of 10 or 14 causes a total voltage measurement to be performed. A function code of 11 or 15 causes a fundamental voltage measurement to be performed. A function code of 12 or 16 causes an in-phase voltage measurement to be performed. A function code of 13 or 17 causes a quadrature voltage measurement to be performed.

One phase of a three phase AC signal is used as a reference voltage for the AC to DC converter. Function codes 25, 26 and 27 determine which phase is used (see Figure 1-3).

(9) Level Detectors

Each of 22 level detectors detect one of three different level changes: open to +28 volts, open to ground and ground to +28 volts. Individual switches are provided to select the level change which is to be detected. Each time a function code 03 is received, the function decode logic provides a signal to gate the outputs of the level detectors into the 22 least significant bits of the output register. If the level has changed, a ONE is entered into the output register flip-flop. A separate indicator is provided on the control panel for each detector.

(10) Alarm Circuits

A total of 22 alarm circuits are provided. Twelve of the circuits (1 through 12) monitor DC voltage levels and the remaining 10 (13 through 22) monitor AC (400 cps) voltage levels. Circuit 1, 2 or 3 provides an output signal if the input voltage is less than 25 or more than 31 volts DC. Circuit 4 provides an output signal if the input voltage is less than 54 or more than 58 volts DC. Any of circuits 5 through 12 provides an output signal if the input voltage is less than 58 or more than 62 volts DC. Circuit 13, 14 or 15 provides an output signal if the input voltage is less than 9.5 or more than 10.5 volts AC. Circuit 16, 17, 18 or 19 provides an output signal if the input voltage is less than 24 or more than 28 volts AC. Circuit 20, 21 or 22 provides an output signal if the input voltage is less than 112.5 or more than 117.5 volts AC.

The detectors are accurate to within 5 percent of the input voltage. The output signals are gated to the 22 least significant bits of the output register when an 04 function code is received. A separate indicator is provided on the control panel for each circuit.

(11) Break Point Switches

Six break point switches on the control panel provide for manually entering data into the six least significant bits of the output register. The information entered into the switches is loaded into the six least significant bits of the output register each time a function code of 20 is received.

(12) Analog-to-Digital Converter

The analog-to-digital converter is a SEL standard Model ADC-1B. The A/D converter converts the analog input voltages from the solid state multiplexer, AC to DC converter or operational amplifier into 14-bit binary words including sign. When a full scale (±10.24 volts) input signal is applied, the converter generates a binary word of ±8191. Each bit represents 1.25 millivolts of the analog input signal. The words are generated in a serial manner with the most significant bit (sign) being generated first. As each bit is generated, it is shifted into the output register. An end of conversion signal is used to generate the "data ready" signal for the computer. The coded words for any one of the multiplexer input channels can be selected for display.

(13) Typewriter

The typewriter is a Friden Flexowriter with a paper tape reader/perforator attachment. The typewriter is used as both an input and output device. When used as an output device, the word contained in the input register or in the output register is gated into the typewriter input/output register and typed out. When used as an input device, manually entered characters from the keyboard are coded and presented to the computer. The typewriter is also used as an input device when the system is being operated in the manual mode. The manual mode operating function is explained in paragraph (4).

When a function code of 23 and an internal sequencer instruction code 1 is received in the input register from the computer, the typewriter control logic switches to an alpha/numeric mode of operation. Subsequent 24-bit words from the computer are gated through the input register into the typewriter input/output register. Each word is loaded into the typewriter buffer register as four 6-bit characters where each character is decoded to type out one alpha/numeric character. Data words are typed out until an end-of-message code is received from the computer. The end-of-message code switches the typewriter control logic back to the octal mode. The end-of-message code is shown in Figure 1-3.

When an internal sequencer instruction code 2 is received with any function code, the desired function is performed and then the 24-bit word in the output register is gated into the typewriter input/output register. The word is gated into the typewriter buffer register as eight 3-bit characters where each character is decoded to type out one octal digit. The word in the output register is also printed out each time the operator selects the r (readout) key on the typewriter when in the manual mode.

When a function code 23 and an internal sequencer instruction code 7 is received in the input register, the typewriter switches to the alpha/numeric mode. The system stops until the operator enters a predetermined message into the typewriter. Each key selection is coded into one 6-bit character and is gated into the typewriter input/output register. After one word (four characters) has been generated, a load command from the typewriter control logic gates the 24-bit word into the output register where it is presented to the computer. After the message has been entered, the operator provides an end-of-message signal by selecting the "/" key. The end-of-message signal is presented to the computer and returns the typewriter control logic to the octal mode.

c. Characteristics

(1)	Modes of Operation	Automatic, single step or manual.
(2)	Input Control Word Length	24 bit.
(3)	Output Data Word Length	24 bit.
(4)	Parity	Odd.
(5)	Analog Inputs:	
	To DC Relay Multiplexer . . .	120 (0 to ±61.44 VDC).
	To AC Relay Multiplexer . . .	60 (153.6 volts RMS).
	To Solid State Multiplexer . . .	64 (0 to ±10.24 VDC).
(6)	Level Inputs (Switch Selectable):	
	Open to +28 Volts Open to Ground Ground to +28 volts }	22 Total.
	Addressing	Program at random.
	Output	To patch panel.
(7)	Alarm Inputs:	
	Quantity	22
	Input Voltages	Refer to paragraph b (10).
	Accuracy	5% of input.
	Threshold Setting	1 volt.
	Addressing	Program at random.
	Output	Gated to output register.
(8)	Signal Output Relays:	
	Quantity	32 (Allied Control)
	Type	3-pole, double throw.
	Switching Time	5 milliseconds.
	Command Signal Time	2 microseconds.
	Dropout Commands	Individual or simultaneous.
	Addressing	Program at random.
	Output	To patch panel.

(9) Recorder Matrix Relays:

Quantity	64 (Allied Control).
Type	3-pole, double throw.
Switching Time	5 milliseconds.
Command Signal Time	2 microseconds.
Output Bussing	8 groups of 8.
Dropout Commands	Individual or simultaneous.
Addressing	Program at random (any one in each group of 8).
Output	To patch panel.

(10) AC Relay Multiplexer:

Number of Input Channels	64 (individually shielded pairs to C. P. Clare relays).
Channel Addressing	Program at random. (5.0 sps maximum).
Input Voltage Ranges (rms)	0 to 1.024 volts. 0 to 10.24 volts. 0 to 51.20 volts. 0 to 153.60 volts.
Input Frequency	350 cps to 5 KC.
Accuracy:	
Zero Offset	0.01 percent.
Crosstalk	0.018 percent.
Noise	0.005 percent.
Linearity	Same as input.
Output	To AC to DC converter.

(11) DC Relay Multiplexer:

Number of Input Channels	120 (individually shielded pairs of Microscan C-2925 relays).
Channel Addressing	Program at random. (400 sps maximum)
Input Voltage Ranges (DC)	0 to ±0.512 volts. 0 to ±1.024 volts. 0 to ±10.24 volts. 0 to ±20.48 volts. 0 to ±61.44 volts.
Accuracy	
Zero Offset	0.001 percent.
Crosstalk	0.018 percent.
Noise	0.005 percent.
Linearity	Same as input.

Output	To operational amplifiers.

(12) Solid State Multiplexer:

Number of Input Channels	64 (individually shielded pairs to SEL 8032 high level gate-Bright switch).
Channel Addressing	Program at random. (10 KC maximum)
Input Voltage Range	±10.24 volts DC.
Input Impedance	Greater than 1 megohm.

Accuracy:

Zero Offset	±0.015 percent.
Linearity	±0.015 percent.
Crosstalk	±0.012 percent.
Gain Error	±0.022 percent.
Noise	±0.02 percent.

Output	To analog-to-digital converter.

(13) AC to DC Converter:

Input Voltages	Refer to AC relay multiplexer input voltages and frequency.
Output Voltage	±10.24 volts with full scale input.
Input Selection	Direct or floating.
Voltage measurement modes	Total voltage. Fundamental voltage. In-phase voltage. Quadrature voltage.
Reference Voltage	Any one of three phases (A, B or C) of 115 vac.
Programmable selections	Gain. Input. Measurement mode. Reference.
Output	To analog-to-digital converter.
Accuracy - Offset	±.1 percent or 10 mv.
Linearity	±.1 percent.
Noise	±.1 percent.

(14) Differential Operational Amplifier

Input Voltages	Refer to DC multiplexer input voltage ranges.
Output Voltage	±10.24 volts with full scale input.
Gain Selection	Program at random except must be same as AC to DC converter if DC multiplexer is commanded before expiration of AC multiplexer sample time.
Input Impedance	Greater than 1.0 megohms.
Maximum Common Mode Voltage	70 volts.
Settling Time	0.200 milliseconds after DC multiplexer relay closure and A/D converter code command.
Output	To analog-to-digital converter.

(15) Analog-to-Digital Converter

Model	SEL ADC-1B.
Input	0 to ±10.24 volts DC.
Output	14-bit binary (including sign).
Resolution	1.25 millivolts/bit.
Bit Rate	200 KC- 500 KC.
Cycle Time (at 200 KC)	100 microseconds (total).
Sample Time	15 Microseconds.
Code Time	80 microseconds.

Accuracy

Zero Offset	0.025 percent.
Linearity	0.02 percent.
Resolution	0.0125 percent.
Gain Error	0.015 percent.

(16) Displays

Level Detectors	22 Amperex (individual).
Alarms	22 Amperex (individual).
Signal Output Relays	32 Amperex (individual).
Recorder Matrix Relays	64 Amperex (individual).
Input Register	8 Nixie (octal).
Output Register	8 Nixie (octal).
Typewriter Register	24 Amperex (individual bit).
A/D Converter Output	14 Amperex (Binary).